3. (amended) The apparatus of Claim 5[1] wherein said output is coupled to a display device.

5. (amended) An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output;

a monitor for monitoring temperature within said apparatus; and

a clock manager adapted to receive a control signal from said monitor, said clock manager selectively stopping clock signals from being sent to said central processing unit (CPU) when said monitored temperature rises to a level at and above a selected reference temperature level and said CPU is not processing [non-]critical I/O.

6. (amended) An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output, said central processing unit (CPU) receiving one of a first clock signal at a first speed or a second clock signal at a second speed; and

a clock manager coupled to a monitor that monitors temperature within said apparatus, said clock manager designating that said central processing unit (CPU) receives said first clock signal when said monitored temperature is at a level below a selected reference temperature level and receives said second clock signal when said detected temperature is at a level at and above said selected reference temperature level and said CPU is not processing critical I/O.

9. (amended) An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output;

a monitor for monitoring temperature within said apparatus; and

a clock manager adapted to receive a control signal from said monitor, said clock manager reducing central processing unit (CPU) clock speed when said detected temperature level is at and above a selected reference temperature level and said CPU is not processing critical I/O.

11. (amended) An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output;

a monitor for monitoring temperature within said apparatus; and

a clock manager adapted to receive a control signal from said monitor, said clock manager reducing central processing unit (CPU) clock speed when said monitored temperature level is at and above said selected reference temperature level and said CPU is not processing [non-]critical I/O.

Cancel Claims 13-16.

17. (amended) A computer, comprising:

means for predicting temperature levels associated with [relevant to] the operation of a central processing unit within said computer; and

means for using said prediction for automatic control of temperature within said computer, said temperature control remaining transparent to a user of said computer.

18. (amended) A computer, comprising:

means for predicting temperature levels associated with the operation of [within] said computer; and

means for using said prediction for automatic temperature control within said computer, said temperature control remaining transparent to a user of said computer.

21. (amended) An apparatus, comprising:

a central processing unit (CPU);

means for sampling a temperature level within said apparatus; and

means for automatically adjusting the processing speed of said central processing unit (CPU) by modifying the clock signal utilized by the central processing unit (CPU) to maintain said temperature level within said apparatus below a selected reference temperature level when said CPU is not processing critical I/O.

Cancel Claims 24-29.

30. (amended) The apparatus of Claim 5[1] wherein said clock manager further stops clock signals from being sent to a PCI bus coupled to the central processing unit (CPU).

Cancel Claims 32 and 33.

36. (amended) The apparatus of Claim 11 [10], wherein said monitor is on board said central processing unit (CPU).

37. (amended) The apparatus of Claim[s 1]6, wherein said monitored temperature is detected via a temperature sensor coupled to said central processing unit (CPU).

40. (amended) The apparatus of Claim 11[0], wherein said monitored temperature is detected via a temperature sensor coupled to said central processing unit (CPU).

71. (amended) The apparatus of Claim 11, wherein said monitor uses a control system of continuous feedback loops.

Cancel Claim 74.

REMARKS

Claims 1, 13-16, 24-29, 32, 33 and 74 are canceled by this amendment.

Claims 2-3, 5-6, 11, 34-35, 37-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67, and 71-73 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hollowell, II et al. in view of Kikinis.

Independent Claim 5, as amended, requires and positively recites, "a provision for user input", "a provision for output", "a central processing unit (CPU) coupled to said user input and output", "a monitor for monitoring temperature within said apparatus", and "a clock manager adapted to receive a control signal from said monitor, said clock manager **selectively stopping clock signals from being sent to said central processing unit (CPU) when said monitored temperature rises to a level at and above a selected reference temperature level and said CPU is not processing critical I/O**".

Independent Claim 6, as amended, requires and positively recites, "a provision for user input", "a provision for output", "a central processing unit (CPU) coupled to said user input and output, said central processing unit (CPU) receiving one of a first clock signal at a first speed or a second clock signal at a second speed" and "a clock manager coupled to a monitor that monitors temperature within said apparatus, said clock manager **designating that said central processing unit (CPU) receives said first clock signal when said monitored temperature is at a level below a selected reference temperature level and receives said second clock signal when said detected temperature is at a level at and above said selected reference temperature level and said CPU is not processing critical I/O."**

Independent Claim 9, as amended, requires and positively recites, "a provision for user input", "a provision for output", "a central processing unit (CPU) coupled to said user input and output", "a monitor for monitoring temperature within said apparatus" and "a clock manager adapted to receive a control signal from said monitor, said clock manager **reducing central processing unit (CPU) clock speed when said detected temperature level is at and above a selected reference temperature level and said CPU is not processing critical I/O**".

Independent Claim 11, as amended, requires and positively recites, "a provision for user input", "a provision for output", "a central processing unit (CPU) coupled to said user input and

output", "a monitor for monitoring temperature within said apparatus" and "a clock manager adapted to receive a control signal from said monitor, said clock manager **reducing central processing unit (CPU) clock speed when said monitored temperature level is at and above said selected reference temperature level and said CPU is not processing critical I/O**".

Independent Claim 21, as amended, requires and positively recites, "a central processing unit (CPU)", "means for sampling a temperature level within said apparatus" and "means for automatically adjusting the processing speed of said central processing unit (CPU) by modifying the clock signal utilized by the central processing unit (CPU) **to maintain said temperature level within said apparatus below a selected reference temperature level when said CPU is not processing critical I/O**".

Applicants agree with the Examiner's analysis of Hollowell as set forth in the Office Action dated October 16, 1997 on page 3, lines 18-23. Applicants also agree with the Examiner that Hollowell does not teach stopping the clock signals when a detected temperature rises above a reference temperature level. Applicants further agree with the Examiner that Hollowell does not teach a monitor stopping the clock signals to the CPU only when the CPU is processing non-critical I/O. While Kikinis teaches that it is known to selectively stop clock signals when the detected temperature rises above a reference temperature level, Kikinis fails to teach or suggest that the selective stopping is performed only when the monitored temperature is at or above a selected reference and said CPU is not processing critical I/O. Indeed, neither Kikinis nor Hollowell teaches or suggests that critical I/O will, or should, affect the performance of the temperature reduction mechanism.

Applicants further submit that it would not be obvious to one of ordinary skill in the art to combine the Kikinis and Hollowell references and thereafter modify the resulting combination device so that the resulting temperature reduction mechanism will selectively stop the clock signal to the CPU only when the monitored temperature is at or above a selected reference and said CPU is not processing critical I/O.

The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Laskowski, 871 F.2d 115, 10 USPQ2d 1397 (Fed. Cir. 1989); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). Simply put, the prior art does not teach or suggest the modifications necessary to attain Applicants' claimed invention. Accordingly, the Examiner has improperly used hindsight and Appellants' disclosure to obviate their claimed invention. It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985). Moreover, "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). The 35 U.S.C. § 103 rejection is overcome.

Claims 2, 3, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67, 71-73 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 2 further defines the apparatus of Claim 5 wherein said user input is coupled to a keyboard.

Claim 3 further defines the apparatus of Claim 5 wherein said output is coupled to a display device.

Claim 34 further defines the apparatus of Claim 5, wherein said monitor is on board said central processing unit (CPU).

Claim 35 further defines the apparatus of Claim 9, wherein said monitor is on board said central processing unit (CPU).

Claim 36 further defines the apparatus of Claim 11, wherein said monitor is on board said central processing unit (CPU).

Claim 37 further defines the apparatus of Claim 6, wherein said monitored temperature is detected via a temperature sensor coupled to said central processing unit (CPU).

Claim 38 further defines the apparatus of Claim 5, wherein said monitored temperature is detected via a temperature sensor coupled to said central processing unit (CPU).

Claim 39 further defines the apparatus of Claims 9, wherein said monitored temperature is detected via a temperature sensor coupled to said central processing unit (CPU).

Claim 40 further defines the apparatus of Claim 11, wherein said monitored temperature is detected via a temperature sensor coupled to said central processing unit (CPU).

Claim 41 further defines the apparatus of Claim 37, wherein said temperature sensor is mounted directly on said central processing unit (CPU).

Claim 42 further defines the apparatus of Claim 38, wherein said temperature sensor is mounted directly on said central processing unit (CPU).

Claim 43 further defines the apparatus of Claim 39, wherein said temperature sensor is mounted directly on said central processing unit (CPU).

Claim 44 further defines the apparatus of Claim 40, wherein said temperature sensor is mounted directly on said central processing unit (CPU).

Claim 45 further defines the apparatus of Claim 37, wherein said temperature sensor is mounted within said central processing unit (CPU).

Claim 46 further defines the apparatus of Claim 38, wherein said temperature sensor is mounted within said central processing unit (CPU).

Claim 47 further defines the apparatus of Claim 39, wherein said temperature sensor is mounted within said central processing unit (CPU).

Claim 48 further defines the apparatus of Claim 40, wherein said temperature sensor is mounted within said central processing unit (CPU).

Claim 49 further defines the apparatus of Claim 37, wherein said temperature sensor is mounted on a printed wiring board (PWB) adjacent said central processing unit (CPU).

Claim 50 further defines the apparatus of Claim 38, wherein said temperature sensor is mounted on a printed wiring board (PWB) adjacent said central processing unit (CPU).

Claim 51 further defines the apparatus of Claim 39, wherein said temperature sensor is mounted on a printed wiring board (PWB) adjacent said central processing unit (CPU).

Claim 52 further defines the apparatus of Claim 40, wherein said temperature sensor is mounted on a printed wiring board (PWB) adjacent said central processing unit (CPU).

Claim 53 further defines the apparatus of Claim 37, wherein said temperature sensor is a thermistor.

Claim 54 further defines the apparatus of Claim 38, wherein said temperature sensor is a thermistor.

Claim 55 further defines the apparatus of Claim 39, wherein said temperature sensor is a thermistor.

Claim 56 further defines the apparatus of Claim 40, wherein said temperature sensor is a thermistor.

Claim 57 further defines the apparatus of Claim 6, wherein said temperature is sensed on a periodic basis.

Claim 58 further defines the apparatus of Claim 5, wherein said temperature is sensed on a periodic basis.

Claim 59 further defines the apparatus of Claim 9, wherein said temperature is sensed on a periodic basis.

Claim 60 further defines the apparatus of Claim 11, wherein said temperature is sensed on a periodic basis.

Claim 61 further defines the apparatus of Claim 57, wherein the frequency of said temperature sensing changes as said temperature reaches preselected threshold values.

Claim 62 further defines the apparatus of Claim 58, wherein the frequency of said temperature sensing changes as said temperature reaches preselected threshold values.

Claim 63 further defines the apparatus of Claim 59, wherein the frequency of said temperature sensing changes as said temperature reaches preselected threshold values.

Claim 64 further defines the apparatus of Claim 60, wherein the frequency of said temperature sensing changes as said temperature reaches preselected threshold values.

Claim 65 further defines the apparatus of Claim 57, wherein the frequency of said temperature sensing is user modifiable.

Claim 66 further defines the apparatus of Claim 58, wherein the frequency of said temperature sensing is user modifiable.

Claim 67 further defines the apparatus of Claim 59, wherein the frequency of said temperature sensing is user modifiable.

Claim 68 further defines the apparatus of Claim 60, wherein the frequency of said temperature sensing is user modifiable.

Claim 69 further defines the computer of Claim 18, wherein said temperature levels are predicted using a temperature prediction mode.

Claim 69 further defines the computer of Claim 18, wherein said temperature levels are predicted using a temperature prediction mode.

Claim 70 further defines the computer of Claim 18, wherein said temperature levels are predicted using a temperature prediction mode without using temperature sensors.

Claim 71 further defines the apparatus of Claim 11, wherein said monitor uses a control system of continuous feedback loops.

Claim 72 further defines the apparatus of Claim 5, wherein said monitor uses a control system of continuous feedback loops.

Claim 73 further defines the apparatus of Claim 9, wherein said monitor uses a control system of continuous feedback loops.

Claims 13-16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hollowell, et al in view of Kikinis and further in view of Smith et al.

Independent 17, as amended, requires and positively recites, "means for predicting temperature levels associated with the operation of a central processing unit within said computer" and "means for using said prediction for automatic control of temperature within said computer, said temperature control remaining transparent to a user of said computer".

Independent Claim 18, as amended, requires and positively recites, "means for predicting temperature levels associated with the operation of said computer" and "means for using said prediction for automatic temperature control within said computer, said temperature control remaining transparent to a user of said computer".

In contrast, none of the cited references, alone or in combination teach or suggest any means for predicting temperatures levels associated with the operation of a CPU or computer. None of the cited references, alone or in combination, teach or suggest any means for using said prediction for automatic temperature control within said computer. Applicants request that the Examiner specifically point out such teaching in the references should he disagree.

As stated previously, the mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Laskowski, 871 F.2d 115, 10 USPQ2d 1397 (Fed. Cir. 1989); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). Simply put, the prior art does not teach or suggest the modifications necessary to attain Applicants' claimed invention. Accordingly, the Examiner has improperly used hindsight and Appellants' disclosure to obviate their claimed invention. It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985). Moreover, "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). The 35 U.S.C. § 103 rejection is overcome.

Claims 19 and 20 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

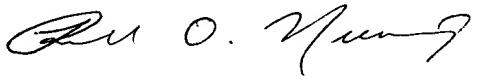
Claim 19 further defines the computer of Claim 17, by including means for user modification of said temperature level predictions.

Claim 20 further defines the computer of Claim 18, including means for user modification of said temperature level predictions.

An amendment after a final rejection should be entered when it will place the case either in condition for allowance or in better form for appeal. 37 C.F.R. 1.116; MPEP 714.12. This amendment places the case in condition for allowance. In any event, this amendment reduces the total number of claims pending and should be entered since it places the case in better form for appeal by reducing the number of issues for appeal.

Claims 2, 3, 5, 6, 9, 11, 16-19, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67 and 71-73 stand allowable and the application is in allowable form. Applicants respectfully request withdrawal of the rejections and allowance of the application.

Respectfully submitted,



Ronald O. Neerings
Reg. No. 34,227
Attorney for Applicants

TEXAS INSTRUMENTS INCORPORATED
P.O. BOX 655474, M/S 3999
Dallas, Texas 75265
Phone: 972/917-5299
Fax: 972/917-4418